2010

MSc—IT

Paper : 2.3

(Computer Organization and Architecture)

Full Marks : 100

Time : 3 hours

The figures in the margin indicate full marks for the questions

1. Choose the correct option : 1×10=10

(a) A shared communication path consisting of one or more connection lines is known as a bus and the transfer of data through this bus is known as

(i) control bus

(ii) data bus

(iii) hypertext transfer protocol

(iv) bus transfer

(b) A microprocessor is a processor with a reduced

(i) power required

(ii) MIPs performance

(iii) instruction set

(iv) None of the above

(c) The group of binary bits assigned to perform a specified operation is known as

(i) control word

(ii) output register

(iii) transfer bus

(iv) None of the above

(d) An ordered collection of items which permits the insertion or deletion of an item to occur only at one end is known as

(i) push

(ii) stack

(iii) pop

(iv) byte

(e) The technique for specifying the address of operands is known as

(i) instruction cycle

(ii) logging

(iii) addressing mode

(iv) complement accumulator

(f) Data is carried along the instruction in

(i) immediate addressing

(ii) direct addressing

(iii) indexed addressing

(iv) None of the above

(g) In instruction cycle

(i) decision phase should precede the fetch phase

(ii) the execute phase always follow the fetch phase

(iii) execute phase and fetch phase are simultaneously executed

(iv) None of the above

(h) The memory system in the computer that is easily read from and written to by the processor is

(i) RAM

(ii) ROM

(iii) ALU

(iv) CPU

(i) A 6 MB program may run in computer system having 4 MB RAM and having

(i) multiprogramming support

(ii) virtual memory support

(iii) multiprocessing support

(iv) None of the above

(j) Cache memory is used in computer system to

(i) ensure fast booting

(ii) replace static memory

(iii) replace hard disk

(iv) speed-up memory access

2. State whether the following statements are True or False : 1×10=10

(a) A program larger than the available main memory size in computer system may run in a PC.

(b) The parallel processing technique increases the computational speed of the processing system.

(c) Static RAM requires periodic refreshing.

(d) In DMA, the data is moved between a peripheral device and the main memory with direct intervention of the processor.

(e) The secondary memory unit does not directly interact with CPU.

(f) When an interrupt occurs, CPU completes the presently executing instruction and then transfers the program control.

(g) Queue is a first-in first-out structure.

(h) PUSH is a zero address instruction.

(i) A strobe is a single-control line that informs the destination unit that a valid data is available on the bus.

(j) The priority is located according to physical position of device in the parallel connection.

(Continued)

3. Fill in the blanks : 1×10=10

(a) The address space is broken into groups of equal size known as —— and the memory space is broken into groups of same size known as ——.

(b) A static RAM is made from an array of ——.

(c) —— is used to support virtual memory.

(d) Daisy chaining is a method to implement ——.

(e) —— transfers data bytes directly from the port to memory location.

(f) —— has to refresh periodically.

(g) —— are events used to stop the current execution and start a new execution.

(h) —— is the technique that identifies the highest priority resource by means of software.

(i) The three major techniques used for transferring data between memory and I/O devices are programmed I/O, interrupt driven I/O and ——.

(j) In case of associative mapping, the contents of the —— memory are not associated with any address.

4. Match Column *A* with Column *B* : 1×10=10

Column A	*Column B*
(a) Stack addressing	*(i)* Relative addressing
(b) Address is an operand	*(ii)* Programmed I/O
(c) Daisy chaining	*(iii)* Register
(d) Virtual memory	*(iv)* Paging
(e) Vector interrupt	*(v)* Output device
(f) Joystick	*(vi)* PUSH and POP
(g) CPU	*(vii)* Interrupt priority
(h) Accumulator	*(viii)* Flip-flop
(i) $R1 \leftarrow R2 + R3$	*(ix)* Input device
(j) Polling	*(x)* Cache memory
	(xi) Immediate addressing
	(xii) Interrupt handler
	(xiii) Control unit
	(xiv) Micro-operation
	(xv) Control operation

5. Answer any *five* from the following : 6×5=30

(a) What is bus? Discuss multiple bus structure with the help of diagrams.

(b) What are two basic memory operations? Discuss them with the help of suitable diagrams.

(c) Discuss different types of computer instructions.

(d) What are the differences between zero-address, one-address and two-address instructions?

(e) What is auxiliary memory? Discuss the construction of a magnetic disk.

(f) Briefly discuss the parallel computer architecture.

(g) What is DMA? Discuss the function of DMA.

6. Answer any *two* from the following : 10×2=20

(a) What do you understand by instruction format? Explain the structure of a typical instruction format.

(b) What is addressing mode? What are different types of addressing mode? Explain with the help of examples.

(c) What do you mean by mapping? Why is it needed? Discuss different types of mapping processes.

(d) Explain what happens when an interrupt occurs. Describe the techniques used in priority interrupt.

7. Write short notes on any *two* of the following : 5×2=10

   (a) Instruction pipeline

   (b) Virtual memory

   (c) Interrupt handling

   (d) Daisy chaining

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